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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/654,920	09/05/2003	Mitsuyoshi Endo	02887.0248	6812

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EXAMINER	
SEMENENKO, YURIY	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 10/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/654,920	ENDO ET AL.	
	Examiner	Art Unit	
	Yuriy Semenenko	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) *13-16* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/2106;8/18/06;12/2/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Amendment filed on 08/21/2006 has been entered.
In response to the Office Action dated 03/21/ 2006, Applicants has amended claims 1, 5 and 12.
Claims 1-16 are now pending in the application.

Specification

2. The Specification amendments, filed on 08/21/2006 are considered and is acknowledged. The Specification amendments are approved.

Claim Objections

3. Claim 5 amendments, filed on 08/21/2006 are considered and is acknowledged. The claims amendments are approved.

Double Patenting

4. The Terminal Disclaimer filled 08/21/2006 approved. Rejection claim 1 on the ground of nonstatutory obviousness-type double patenting have been withdrawn.

Response to Arguments

5.1. Applicant's arguments with respect to independent claim 1 are considered and acknowledged but they are not persuasive.

First of all Applicant cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Merck & Co., Inc., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Applicant argues that references do not discloses an insulating substrate with a porous structure including continuous pores. However, Sakamoto teaches the insulating structure with porous 104, Fig. 1 and Ohya patent clearly demonstrates insulating substrate (base board for printing wiring (column 1, lines 10-15) with a porous structure including continuous pores (Ohya, Abstract, line 3).

Applicant amended claim 1 to introduce "wiring conductors selectively formed in the pores". However, this limitation is a process limitation in the product claim. Such a process limitation defines the claimed invention over the prior art only to the degree that it defines the product itself. A process limitation cannot serve to patentably distinguish the product over the prior art, in the case that the product is the same as, or obvious over, the prior art. See Product-by-Process in MPEP 2113 and 2173.05(p) and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985).

Further, if the prior art structure (insulating substrate with porous structure and wiring conductors) is capable of performing the intended use (connect an electronic device to electronic module), then it meets the claim. See In re Casey, 152 USPQ 235 (CCPA 1967) AND In re Otto, 136 USPQ 458, 459 (CCPA 1963).

Examiner notes that it is a common knowledge to consider connection of an electronic device to a wiring conductors by pads, lands or bumps as directly connections. Such connection clearly shown on Fig. 8F (Okubora).

5.2. Applicant's arguments with respect to dependent claims 2-12 are considered and acknowledged but they are not persuasive as based on arguments with respect to independent claim 1 as discussed above.

5.3. Examiner apologizes for typographical error in previous Office Action.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6.1. Claim 1 is rejected under 35U.S.C. 103(a) as being obvious over Okubora in view of Sakamoto et al. (Patent #5103288 hereinafter "Sakamoto") and in view of Ohya et al. (Patent #5531945 hereinafter "Ohya").

As to claim 1: Okubora discloses in Fig. 8F an electronic device module comprising: a wiring substrate 43, Fig. 8B having an insulating substrate (41, Fig. 8 and column 5, lines 18-22) and wiring conductors 43b, 44, Fig. 8F selectively formed in substrate; and an electronic device 50 directly connected to said wiring conductors formed in the substrate.

except , Okubora doesn't explicitly teach a substrate with a porous structure.

Sakamoto discloses a substrate with a porous structure (column 2, lines 65-68

and column 3, lines 1-9).

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention that a substrate with a porous structure as taught by Sakamoto because Sakamoto teaches that such structure would result in the benefit of reducing the parasitic capacitance.

However, Okubora doesn't explicitly teach a porous structure including continuous pores.

Ohya teaches a porous structure including continuous pores.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention that a porous structure including continuous pores, as taught by Ohya because Ohya teaches that such structure would result in the benefit of forming a printed wiring network.

Instant modified Okubora clearly teaches all of the claimed limitations. Applicant amended claim 1 to introduce "wiring conductors selectively formed in the pores". However, this limitation is a process limitation in the product claim. Such a process limitation defines the claimed invention over the prior art only to the degree that it defines the product itself. A process limitation cannot serve to patentably distinguish the product over the prior art, in the case that the product is the same as, or obvious over, the prior art. See Product-by-Process in MPEP 2113 and 2173.05(p) and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985).

Further, if the prior art structure ((Okubora as modified, disclosed insulating substrate with porous structure and wiring conductors) is capable of performing the intended use (connect an electronic device to electronic module), then it meets the claim. See In re Casey, 152 USPQ 235 (CCPA 1967) AND In re Otto, 136 USPQ 458, 459 (CCPA 1963).

6.2 Claims 1-4, 6 and 8-9 are rejected under 35U.S.C. 103(a) as being obvious over of Okubora in view Admitted by Applicant (Prior Art, hereinafter APA) .

As to claim 1: Okubora discloses in Fig. 8F an electronic device module comprising: a wiring substrate 43, Fig. 8B having an insulating substrate (41, Fig. 8 and column 5, lines 18-22) and wiring conductors 43b, 44, Fig. 8F selectively formed in substrate; and an electronic device 50 directly connected to said wiring conductors substrate.

except , Okubora doesn't explicitly teach a substrate with a porous structure including continuous pores.

APA discloses at time the invention was made, it was well know to use a three-dimensional structure of the substrate including continuous pores (Specification, page 2, lines 1-9).

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention that a substrate with a porous structure including continuous pores as taught by APA because APA teaches that such structure would result in the benefit of stereoscopic wiring board with high degree of freedom in circuit design.

Instant modified Okubora clearly teaches all of the claimed limitations. Applicant amended claim 1 to introduce "wiring conductors selectively formed in the pores". However, this limitation is a process limitation in the product claim. Such a process limitation defines the claimed invention over the prior art only to the degree that it defines the product itself. A process limitation cannot serve to patentably distinguish the product over the prior art, in the case that the product is the same as, or obvious over, the prior art. See Product-by-Process in MPEP 2113 and 2173.05(p) and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985).

Further, if the prior art structure ((Okubora as modified, disclosed insulating substrate with porous structure and wiring conductors) is capable of performing the intended use (connect an electronic device to electronic module), then it meets the claim. See In re Casey, 152 USPQ 235 (CCPA 1967) AND In re Otto, 136 USPQ 458, 459 (CCPA 1963).

As to claim 2: Okubora discloses the electronic device module according to claim 1, wherein said wiring conductors in the wiring substrate are grouped into a first wiring

conductor 43a, 43b extending in parallel with a electronic device mounting surface of the porous insulating substrate (41, Fig. 8 and column 5, lines 18-22) and a second wiring conductor 44 extending through the porous insulating substrate from its top surface to bottom surface, Fig. 8B. We consider through hole 44 as a second wiring conductor because as taught by Okubora via-holes which are metal plated at the inner wall to give a level of conductivity or filled with an electrically conductive paste for yielding the via holes to connect between the patterns in layers (column 8, lines 40-49).

As to claim 3: Okubora discloses the electronic device module according to claim 2, wherein said first wiring conductor 72 Fig. 9E is formed at a surface of said wiring substrate 71.

As to claim 4: Okubora discloses the electronic device module according to claim 2, wherein said first wiring conductor (71a, 71b Fig. 9A and column 8, lines 51-55) is embedded in said wiring substrate 71.

As to claim 6: Okubora discloses the electronic device module having all of the claimed features as discussed above with respect claim 1, wherein the wiring substrate 49 and the electronic device 50 are directly connected with each other by bonding layers provided at contacts of the wiring conductors 44p with terminal electrodes 51 of the electronic device 50 Fig.8E.

As to claim 8: Okubora discloses the electronic device module according to claim 1, wherein a size of the electronic device 50 is smaller than the size of the wiring substrate 49, Fig.8E.

As to claim 9: Okubora discloses the electronic device module according to claim 1, wherein the insulating substrate 49 has almost the same coefficient of thermal expansion as that of the electronic device 50, (column 7, lines 36-49 column 11, lines 37-42)

6.3. Claim 5 is rejected under 35U.S.C. 103(a) as being obvious over Okubora in view of APA, as applied to claims 1 and 2 above, and further in view of Shibasaki et al. (Patent #4296424 hereinafter "Shibasaki").

As to claim 5: Okubora discloses the electronic device module having all of the claimed features as discussed above with respect claim 2, wherein, in a junction of the first 43a and second wiring conductors defined as planes in parallel with the electronic device 50 mounting surface of the wiring substrate, Fig. 8F,

except, Okubora doesn't explicitly teach the second wiring conductor along the longer extension of the first wiring conductor is greater than that along the shorter extension of the first wiring conductor.

Shibasaki discloses the second wiring conductor 3, 5a, 5b, Fig. 3 along the longer extension of the first wiring conductor is greater than that along the shorter extension of the first wiring conductor. Shibasaki teaches (column 4, lines 27-41) the insulation substrate 1, Fig. 3, includes a photosensitive layer 2 that is, upon exposure to irradiated energy rays, exhibit conductive properties and forms electrodes. At time the invention was made, it was well know how to create conductors from photosensitive layer and that second wiring conductor along the longer extension of the first wiring conductor is greater than that along the shorter extension of the first wiring conductor.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention that the second wiring conductor along the longer extension of the first wiring conductor is greater than that along the shorter extension of the first wiring conductor to provide compound module.

6.4. Claim 7 is rejected under 35U.S.C. 103(a) as being obvious over Okubora in view of APA, as applied to claim 1 above, and further in view of Yasuda et al. (Patent 2002/0100610 hereinafter "Yasuda").

As to claim 7: Okubora discloses the electronic device module having all of the claimed features as discussed above with respect claim 1,

except, Okubora doesn't explicitly teach a size of the electronic device and a size of the wiring substrate are substantially the same.

Yasuda discloses in Fig. 4A a size of the electronic device 5 and a size of the wiring substrate 6 are substantially the same. At time the invention was made, it was well know to use
so-called chip size package (CSP), when a size of the electronic device and a size of the wiring substrate are substantially the same.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention a size of the electronic device and a size of the wiring substrate are substantially the same.

Benefit of doing so is to reduce size of the semiconductor devices.

6.5. Claims 10, 11 are rejected under 35U.S.C. 103(a) as being obvious over Okubora in view of APA, as applied to claim 1 above, and further in view of Japp et al. (Patent #6722031, hereinafter "Japp")

As to claim 10: Okubora discloses the electronic device module having all of the claimed features as discussed above with respect claim 1,

except, Okubora doesn't explicitly teach the electronic device is of semiconductor chip, and the wiring substrate serves as a package base on which the semiconductor chip is mounted.

Japp discloses the electronic device is of semiconductor chip 160, Fig. 2, and the wiring substrate 1020 serves as a package base on which the semiconductor chip is mounted. At time the invention was made, it was well know to use the wiring substrate serves as a package base on which the semiconductor chip is mounted.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention the electronic device is

of semiconductor chip, and the wiring substrate serves as a package base on which the semiconductor chip is mounted .

Benefit of doing so is to prevent damage of the chip and provide necessarily connections.

As to claim 11: Okubora discloses the electronic device module having all of the claimed features as discussed above with respect claim 10,

except, Okubora doesn't explicitly teach the semiconductor chip that is mounted on a top surface of the package base, with its terminal electrodes facing downwards, and a part of the wiring conductors of the package base are directly coupled to the semiconductor chip, and other
part of the wiring conductors extend to a bottom side of the package base.

Japp discloses in Fig. 2 the semiconductor chip 160 that is mounted on a top surface of the package base 1020, with its terminal electrodes 107 facing downwards, and a part of the wiring conductors 103 of the package base 1020 are directly coupled to the semiconductor chip 160, and other part of the wiring conductors 1006, 1008 extend to a bottom side of the package base. At time the invention was made, it was well know the semiconductor chip that is mounted on a top surface of the package base, with its terminal electrodes facing downwards.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention the semiconductor chip that is mounted on a top surface of the package base, with its terminal electrodes facing downwards, and a part of the wiring conductors of the package base are directly coupled to the semiconductor chip, and other part of the wiring conductors extend to a bottom side of the package base.

Benefit of doing so is to provide connections of the chip with another printed circuit board.

6.6. Claim 12 is rejected under 35U.S.C. 103(a) as being obvious over Okubora

in view of APA, as applied to claim 1 above, and further in view of Japp and in view of Hur (Patent #6646334, hereinafter "Hur")

As to claim 12: Okubora discloses the electronic device module having all of the claimed features as discussed above with respect claim 10,

except, Okubora doesn't explicitly teach the semiconductor chip that is mounted on a bottom surface of the package base, with its terminal electrodes facing upwards.

Hur teaches the electronic device is of semiconductor chip that is mounted on a bottom surface of the package base with its terminal electrodes facing upwards. Therefore, at time the invention was made, it was well know the electronic device is of semiconductor chip that is mounted on a bottom surface of the package base with its terminal electrodes facing upwards.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention the semiconductor chip that is mounted on a bottom surface of the package base with its terminal electrodes facing upwards.

Benefit of doing so is to provide possibility to use both sides of the substrate.

Okubora also fail to discloses that a part of the wiring conductors of the package base are directly coupled to the semiconductor chip, and other part of the wiring conductors extend at the bottom surface of the package base.

Japp discloses in Fig. 2 the semiconductor chip 160 that is mounted on a surface of the package base 1020,and a part of the wiring conductors 103 of the package base 1020 are directly coupled to the semiconductor chip 160, and other part of the wiring conductors 1006, 1008 extend to a bottom side of the package base. At time the invention was made, it was well know that a part of the wiring conductors of the package base are directly coupled to the semiconductor chip, and other part of the wiring conductors extend at the bottom surface of the package base.

Therefore it would have been obvious to one of ordinary skill in the art, at time the invention was made, for Okubora to include in his invention the electronic device is of semiconductor chip that is mounted on a bottom surface of the package base, with

its terminal electrodes facing upwards, and a part of the wiring conductors of the package base are directly coupled to the semiconductor chip, and other part of the wiring conductors extend at the bottom surface of the package base.

Benefit of doing so is to provide connections of the chip with another printed circuit board.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yuriy Semenenko whose telephone number is (571) 272-6106. The examiner can normally be reached on 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean A. Reichard can be reached on (571)- 272-2800 ext. 31. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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10/16/06